

40V N-Channel Enhancement Mode Power MOSFET

Description

WMB090N04LG2 uses Wayon's 2nd generation power trench MOSFET technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications.

Features

- $V_{DS} = 40V$, $I_D = 50A$
 $R_{DS(on)} < 9m\Omega$ @ $V_{GS} = 10V$
 $R_{DS(on)} < 15m\Omega$ @ $V_{GS} = 4.5V$
- Low $R_{DS(on)}$
- Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available

Applications

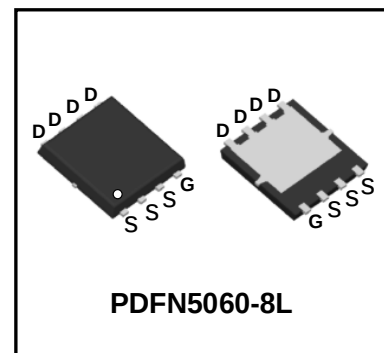
- Power Management in Switches
- DC/DC Converter

Absolute Maximum Ratings ($T_A = 25^\circ C$, unless otherwise noted)

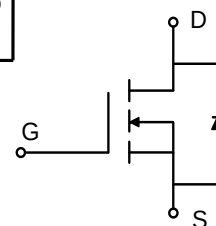
Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ C$	I_D	50	A
	$T_C = 100^\circ C$		33	
Pulsed Drain Current ¹		I_{DM}	200	A
Single Pulse Avalanche Energy ²		EAS	16.2	mJ
Total Power Dissipation	$T_C = 25^\circ C$	P_D	32.9	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ³	$R_{\theta JA}$	56	$^\circ C/W$
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	3.8	$^\circ C/W$



RoHS
compliant



Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	40	-	-	V
Gate-body Leakage Current		I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T _J =25°C	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V	-	-	1	μA
	T _J =100°C			-	-	100	
Gate-Threshold Voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.6	2.5	V
Drain-Source on-Resistance ⁴		R _{DS(on)}	V _{GS} = 10V, I _D = 12A	-	6	9	mΩ
			V _{GS} = 4.5V, I _D = 10A	-	9	15	
Forward Transconductance ⁴		g _{fs}	V _{DS} = 5V, I _D =10A	-	34	-	S
Dynamic Characteristics ⁵							
Input Capacitance		C _{iss}	V _{DS} = 20V, V _{GS} = 0V, f = 1MHz	-	772	-	pF
Output Capacitance		C _{oss}		-	233	-	
Reverse Transfer Capacitance		C _{rss}		-	38	-	
Gate Resistance		R _G	f = 1MHz	-	2.1	-	Ω
Switching Characteristics ⁵							
Total Gate Charge		Q _g	V _{GS} = 4.5V, V _{DS} = 20V, I _D = 12A	-	6.5	-	nC
Gate-Source Charge		Q _{gs}		-	3.2	-	
Gate-Drain Charge		Q _{gd}		-	1.3	-	
Turn-on Delay Time		t _{d(on)}	V _{GS} = 10V, V _{DD} = 20V, R _G = 3Ω, I _D = 12A	-	14.2	-	ns
Rise Time		t _r		-	5.5	-	
Turn-off Delay Time		t _{d(off)}		-	19.5	-	
Fall Time		t _f		-	10.8	-	
Body Diode Reverse Recovery Time		t _{rr}	I _F =12A, di/dt=100A/μs	-	19	-	ns
Body Diode Reverse Recovery Charge		Q _{rr}		-	5	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ⁴		V _{SD}	I _S = 1A, V _{GS} = 0V	-	-	1.2	V
Continuous Source Current	T _C =25°C	I _S	-	-	-	50	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.1\text{mH}, I_{AS} = 18A$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

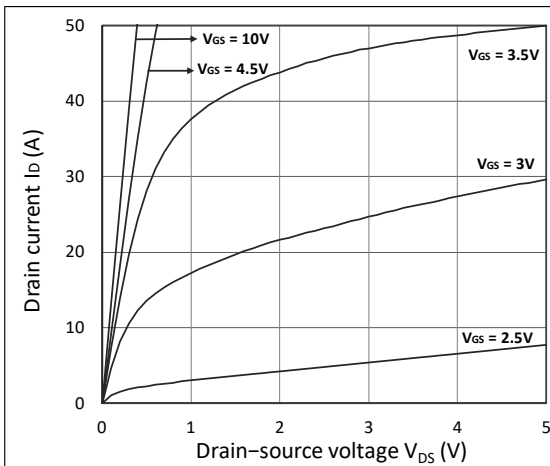


Figure 1. Output Characteristics

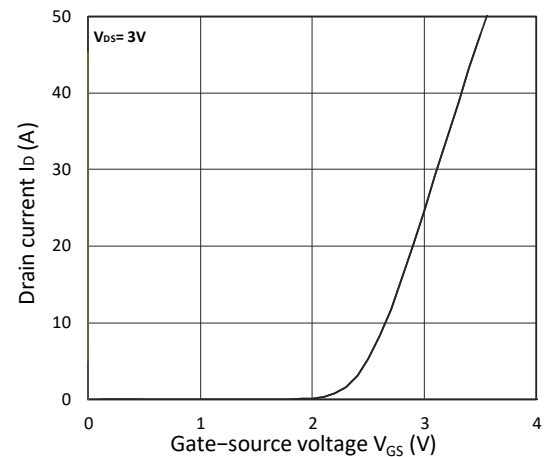


Figure 2. Transfer Characteristics

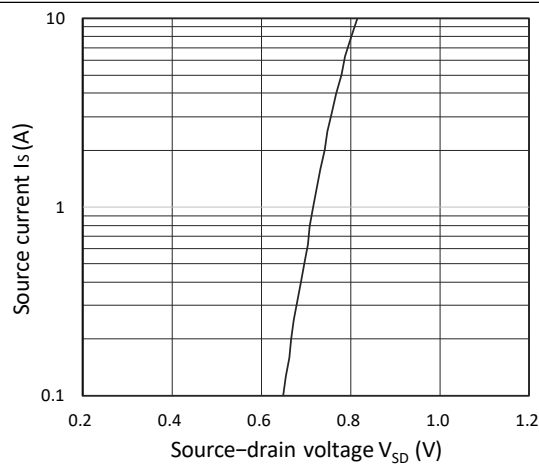
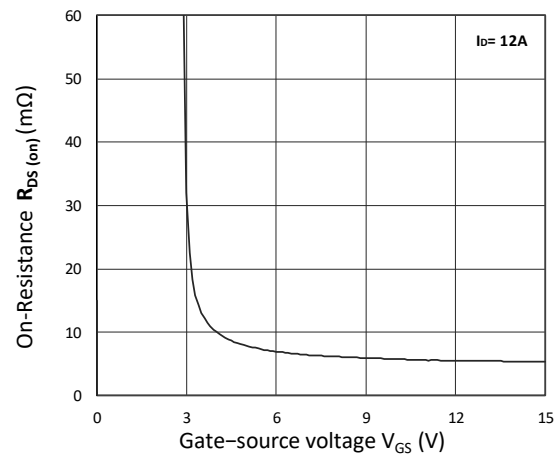
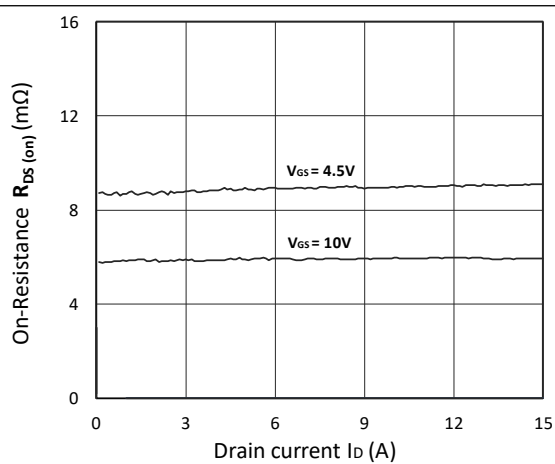
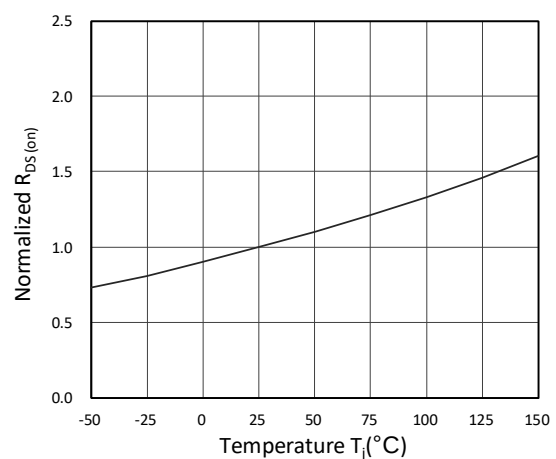


Figure 3. Forward Characteristics of Reverse

Figure 4. $R_{DS(on)}$ vs. V_{GS} Figure 5. $R_{DS(on)}$ vs. I_D Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

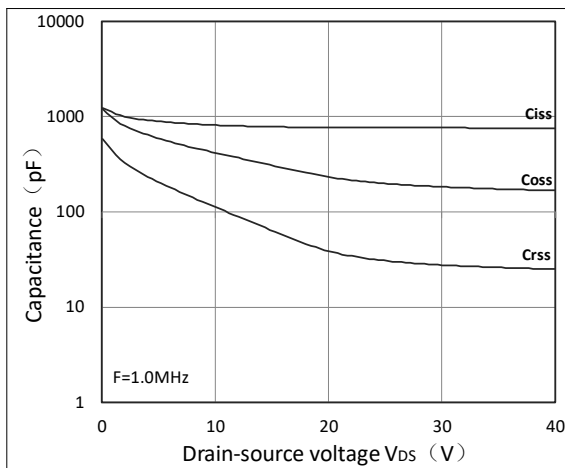


Figure 7. Capacitance Characteristics

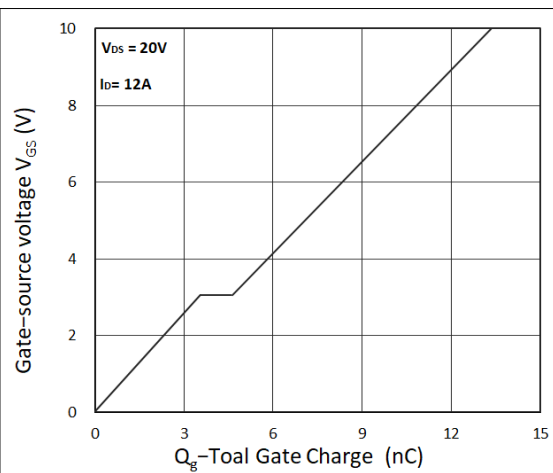


Figure 8. Gate Charge Characteristics

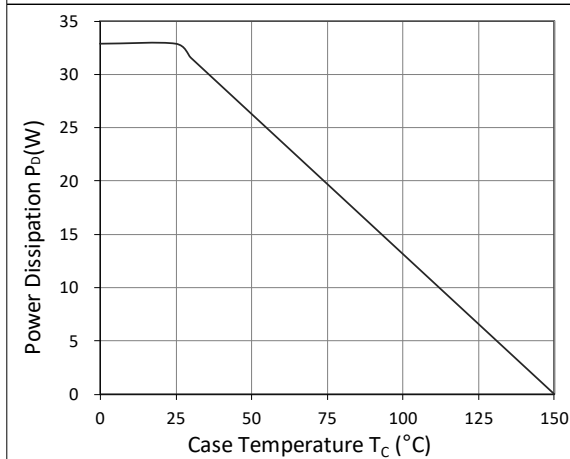


Figure 9. Power Dissipation

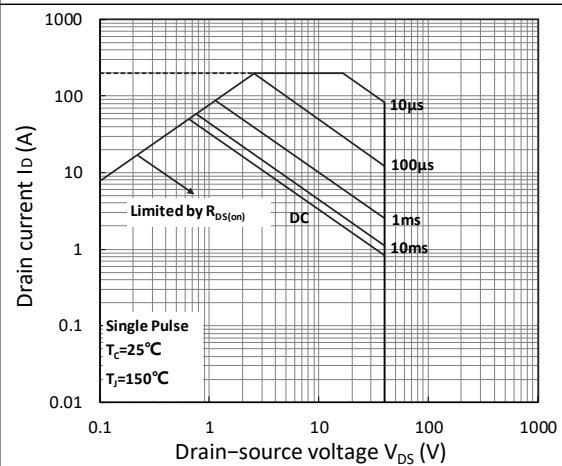


Figure 10. Safe Operating Area

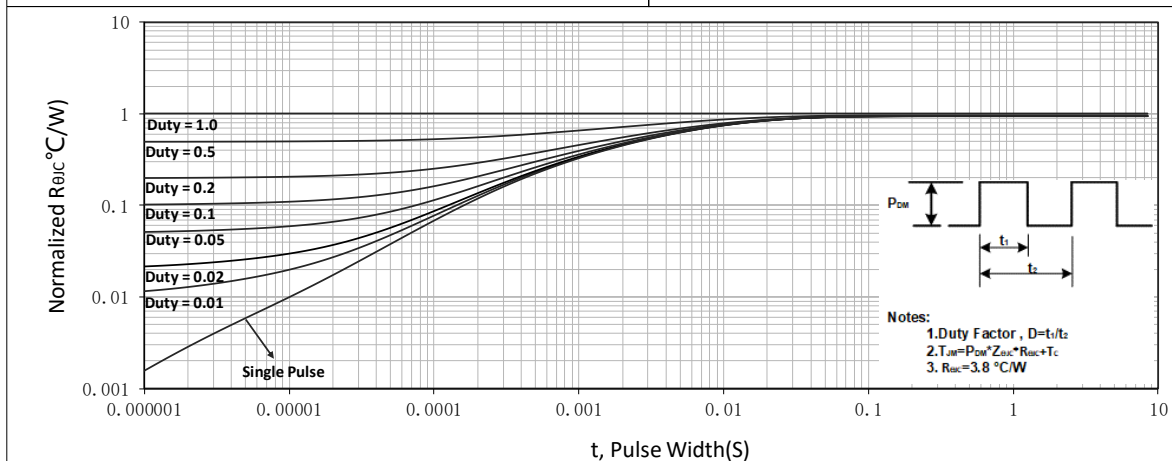


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

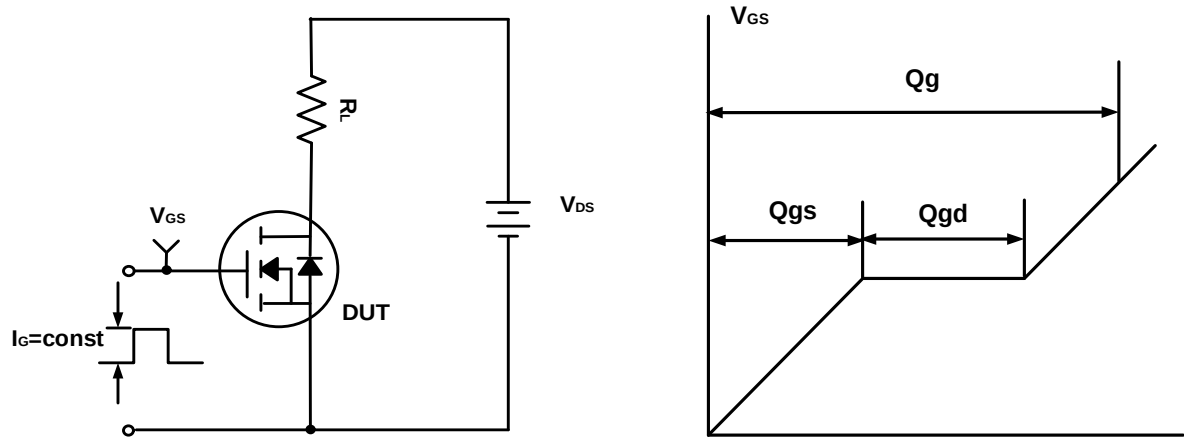


Figure A. Gate Charge Test Circuit & Waveforms

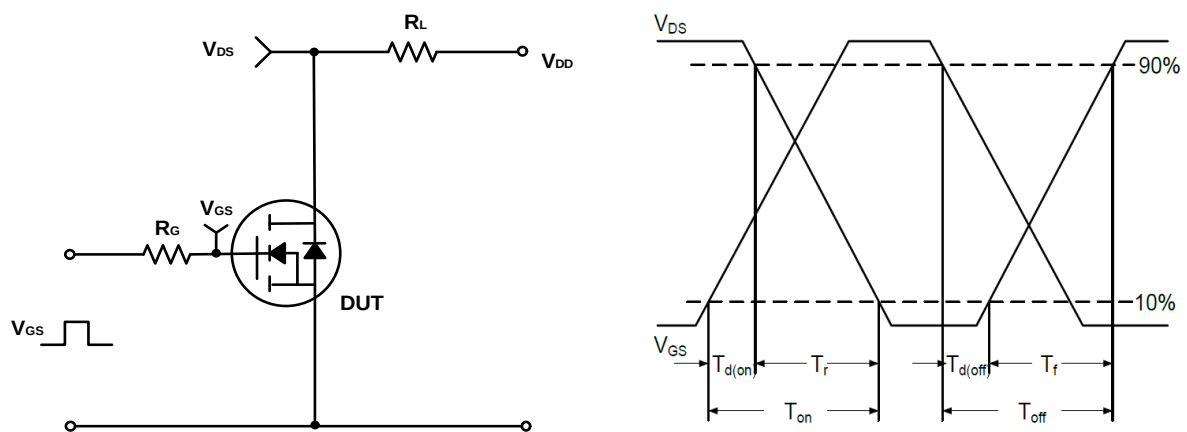


Figure B. Switching Test Circuit & Waveforms

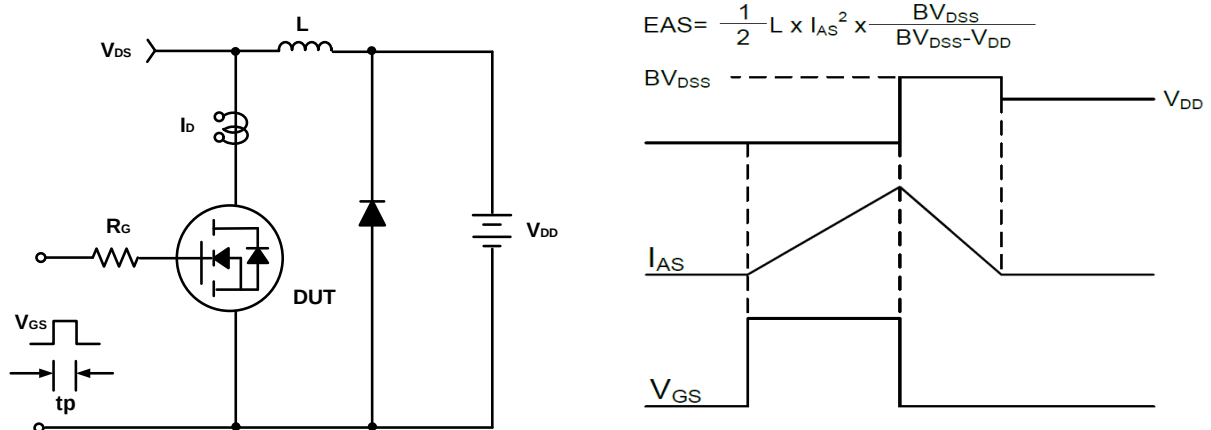
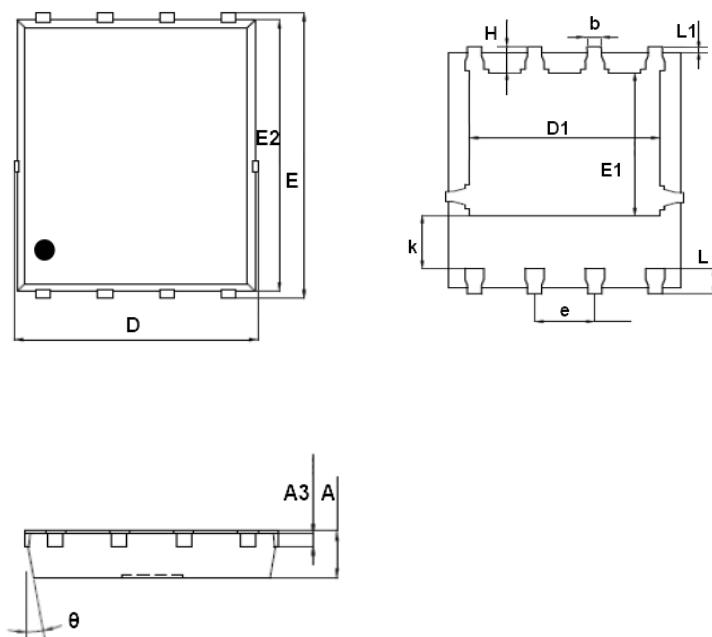


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Mechanical Dimensions for PDFN5060-8L

COMMON DIMENSIONS

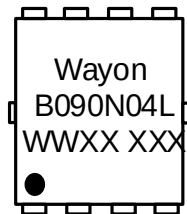


SYMBOL	MM	
	MIN	MAX
A	0.90	1.20
A3	0.15	0.35
D	4.80	5.40
E	5.90	6.35
D1	3.61	4.31
E1	3.30	3.92
E2	5.50	6.06
k	1.10	-
b	0.30	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.71
θ	0°	12°

Ordering Information

Part	Package	Marking	Packing method
WMB090N04LG2	PDFN5060-8L	B090N04L	Tape and Reel

Marking Information



B090N04L = Device code

WWXX XXX= Date code

Contact Information

No.1001, Shiwan(7) Road, Pudong District, Shanghai, P.R.China.201207

Tel: 86-21-50310888 Fax: 86-21-50757680 Email: market@way-on.com

WAYON website: <http://www.way-on.com>

For additional information, please contact your local Sales Representative.

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